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Research Article

Modelling, Simulation and Analysis of Three Phase/Level Vienna Rectifier as a Front end Converter

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A three-stage ac to dc-based Vienna Rectifier with phase three / level bidirectional switch topology is presented here. The various topology of the Vienna Rectifier was analyzed and selected the top topology selection at the low end of Low Harmonic Electric was reported. A comparative study was conducted among the top topology in terms of the number of devices using semiconductor devices, semiconductor losses, number of gate drivers, etc. The Vienna Rectifier topology1 six switches is found to be the best harmonic reduction solution at the end of the Low harmonic Drives. The power circuit design is designed for a 90 kW drive and a Hysteresis-based loop control strategy is implemented. The simulation was applied to the Vi LAB / SIMULINK of the Vienna Rectifier 90 kW at an input voltage of 400 V, 50 Hz, and the dc-link voltage is maintained at 591V (3% boost in line peak voltage). The simulation result shows that sinusoidal input current, unity power factor is achieved and the current THD is limited to less than 5% as normal for IEEE 519-2014.

Keywords: Vienna Rectifier, three level converters, Topologies, Hysteresis control, Power Circuit Design, THD and Power loss.

1. Introduction

Generally, ac-to-dc power converters can be divided into two types such as a modified line also called a performance modifier, and an automatic modifier is known as active or Pulse Width Modulation (PWM). Synthetic modifiers, using a diode or thyristor-based switches, cross the line or switch when zero-frequency current is used while Active Rectifiers hire Active Rectifiers specialists, such as Insulated Gate bipolar transistor (IGBT), Gate Turn-off Thyristor able Consulate (GTO), Thyristor (IGCT), capable of effectively controlling ac supply currents [1].

Non-invasive fixers are less expensive, more reliable, and provide better performance but often inject a significant amount of current harmonics on the supply side and require additional filtering requirements to achieve a coherent strength factor, and do not meet energy quality standards. On the other hand, Functional Fixers are more expensive, less reliable and less efficient compared to synthetic fixers [3]. However, Active Corrections are very promising in terms of energy quality, as a component of cohesiveness and a relatively low current Total Harmonic Distortion (THD) can be achieved.

Vienna rectifier is a three-level non-regenerative three-level booster/level and is the best choice in terms of energy loss, idle size, efficiency, reliability, high power density, low-voltage pressure, component strength, and low power THD meets International Electro-Technical Commission 61000-3-2 / 61000-3-4 guidelines [4]. The factors listed above make the

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Vienna Rectifier an ideal topology for medium and high power consumption [2].

90 kW design, Vienna rectifier phase three / level used showing sinusoidal input power, less than 5% current harmonic distortion on the supply side, and the power element of the joint. Various Vienna rectifier themes, comparisons with top selection options, and power circuit design that includes a well-designed design process, device selection, control method, Inductor selection, and losses are presented.

2. Topologies of Vienna Fixer

The Vienna fixer is taken from a series of connected diode bridge connectors and dc-to-dc converters. Figure 1 shows the basic topology of the Vienna fixer. The leg of each phase consists of six fast-recovery diodes (D1-D6), six line-frequency diodes (Da-Df), and six switches (Sa-Sf).

Chen et al [12] proposed a method to study the multi-dimensional features in each area of the pixels in a flexible manner. The modern semantic image separation model is used for integrated training of input images in multiple scales without the attention model. Also, with the extra monitoring of output on all scales, it is important to get outstanding performance after the integration of multiple scale features. Three interesting data sets, consisting of PASCAL-Person-Part, PASCAL VOC 2012, and the sub-set of MS-COCO 2014 were used to demonstrate model performance by performing extensive tests.

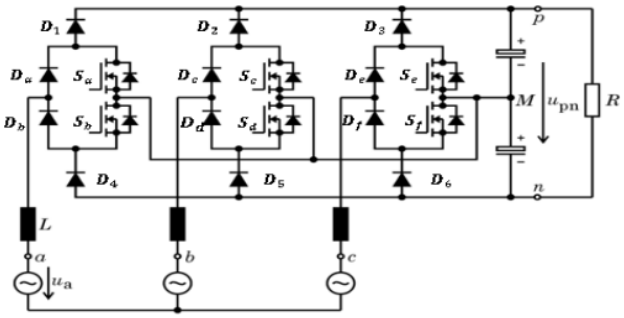

Fig. 1. Topology 1

Alternate phase leg implementations of Vienna Rectifier are shown in Figure 2.

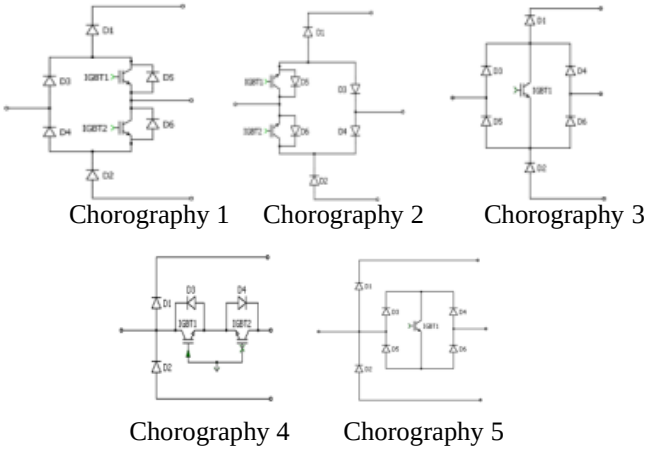

Fig. 2. Various Topologies of Vienna Rectifier

Table 1: Comparison among various Topologies of Vienna Rectifier

S.No	Parameter		Chorography 1	Chorography 2	Chorography 3	Chorography 4	Chorography 5
1	No of diodes		12	12	18	6	18
2	No of IGBT's (S_a)		6	6	3	6	3
3	Total Device count		18	18	21	12	21
4	Blocking voltage of diodes	recovery	Vdc/2	Vdc/2	Vdc/2	Vdc/2	Vdc/2
		frequency	-	-	Vdc/2	-	Vdc/2
5	Blocking energy of switches		Vdc/2	Vdc/2	Vdc/2	Vdc/2	Vdc/2
6	No. of Gate drivers / phase leg		2	2	1	1	1
7	Hardware Realization		Moderate	Moderate	Difficult	Less	Difficult
8	No. of stray inductances in commutation loop		4	4	5	4	5
9	Over voltage spikes		Less	Less	more	Less	More
10	+ive /-ive clamping path		Diode *2	Diode + MOSFET	Diode *2	Diode	Diode *2
11	Middle point clamping path		Diode + MOSFET	Diode + MOSFET	Diode*2+MOSFET	MOSFET *2	Diode*2+MOSFET
12	Devices in commutation		Ex.Diode + MOSFET	Ex.Diode + MOSFET	Ex.Diode + MOSFET	Ex.Diode + MOSFET	Ex.Diode + MOSFET

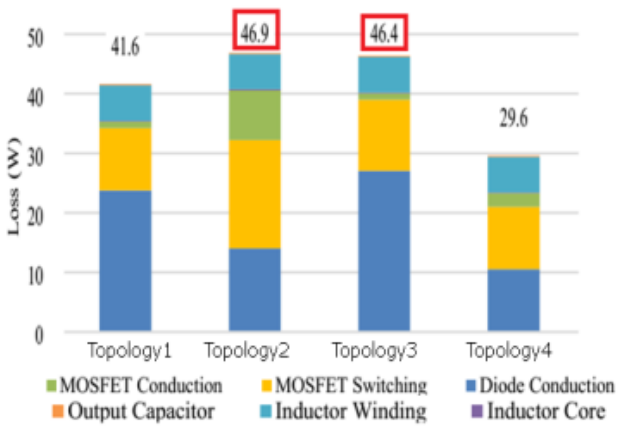

Fig. 3. Loss Comparison

From Figure 3, the losses on topology 2 and 3 are higher. Topology 5 is similar to Topology 3 but the two diodes D1 & D2 on each leg are limited to total DC power output, whereas in topology 3 these are limited to the DC component. Outgoing voltage. So, the loss in Topology 5 is usually higher than Topology3. Finally, topologies 2, 3, and 5 were completed and the topology 1 & 4 were considered for further analysis [5], [1].

3. Power Circuit Design.

The specification of the phase 3 design, which redesigns 3 levels, is shown in Table 2. The input current concepts to be pure sinusoid and a 98% efficiency efficient UPF efficiency.

Table 2: Specifications

Quantity	Rating
DC power output	90 kW
Input 3Ø AC voltage line input	(380-15% of 380) to (500+10% of 500) V
Input voltage frequency	50 Hz
Switching Frequency	20 kHz
Outgoing DC voltage	591 V (1.03*Vline peak)

3.1. Design process

The design process is illustrated with diagrams in the flow chart in Figure 4. Initially, the details of the converter are described following the selection of the modulation system. To find the right design a sweeping system is used. All idle devices such as input boost inductors, DC bus capacitors are designed (especially suppressed by the quality level of power) and their rate of loss of performance and switching loss is calculated based on the choice of switching frequency. This semiconductor device selection that gains low losses will be a design tailored to this variability. By sweeping different exchange frequencies, a correlation between the adjusted size of the idle and losses can be obtained [4].

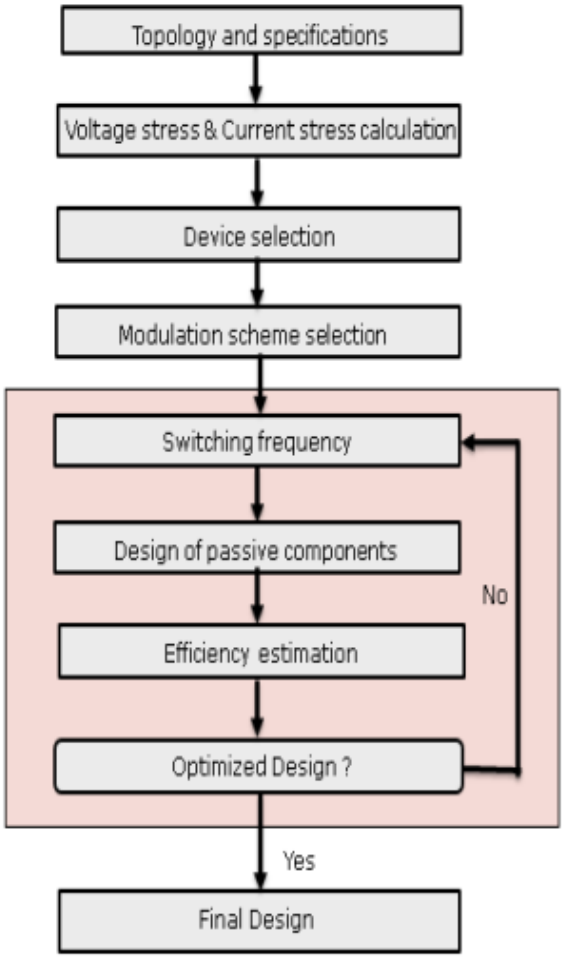

Fig.4. Optimization Procedure

2.1. Device Selection

Mechanical pressure of the machine is calculated by considering the maximum input voltage i.e., 500 + 10% of 500 hence, therefore, V = 550 V. In both topology topics, IGBT electrical pressure is part of the DC output. The electrical pressure of the diodes in topology 1 is half DC output and for topology 4, diodes D1 & D2 are limited to full DC output and D3 and D4 are limited to the DC output phase [6].

The current maximum industrial load over 90 kW is 212 A. The current pressure of the devices is calculated by considering the maximum current overload capacity. The selection of the Topology 1 & 4 devices is shown in Table 3.

Table 3: Device Selection

Parameter	Topology1		Topology4		
	IGBT	D1 – D4	IGBT	D1 & D2	D3 & D4
Voltage Stress(V)	481	481	481	962	481
Voltage Rating(V)	650	650	650	1200	650
Current Stress (A)	330	330	330	330	330
Current Rating(A)	400	400	400	400	400
Module	F3L400R07ME4_B22		F3L400R12PT4_B26		

2.2. Control Technique

A hysteresis-based control strategy is used for phase 3, Rectifier level 3 and is shown in Figure 5. Output controller output and wave formation of input line current are done using individual hysteresis controllers [7], [8]]. The output of the power element of the current organizational index is obtained by the output of the voltage regulator G (s) by the sine wave of unit amplitude and in phase by the input voltage is given in Figure(1).

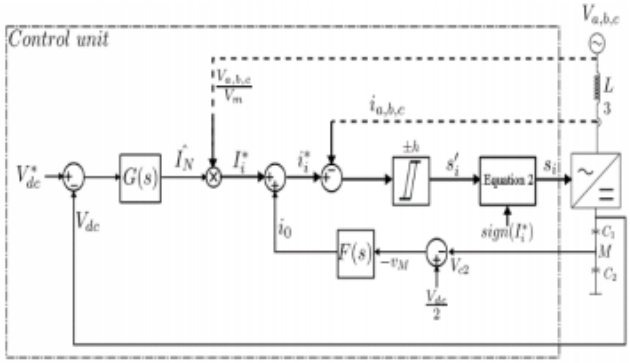

Fig.5. Hysteresis based control strategy

$$I_i^* = I_N \frac{V_{i(i=a,b,c)}}{V_m} \quad (1)$$

To generate control signals, the dependence of the rectifier input volume on the current input signal is considered to be modified as given in Figure (2).

$$S_i = \begin{cases} S_i' & if\ i_i^* \geq 0 \\ NOT\ S_i' & if\ i_i^* < 0 \end{cases} \quad (2)$$

The control of the mains current is obtained by controlling the voltage difference across the inductor (L). The error in the current control is limited to double the number of the hysteresis band (2h) and the IGBT switch signals obtained from the figures (3).

$$S_i' = \begin{cases} 0 & if\ i_i \geq i_i^* + h \\ 1 & if\ i_i < i_i^* - h \end{cases} \quad (3)$$

In addition to controlling the mains current, the voltage rating of the DC bus is also important for all capacitors C1 and C2. The power imbalance of the DC bus is due to the neutral position of the DC M bus neutral at low-frequency AC current and this is reflected in the voltage difference across all capacitors as given in Figures (4).

$$v_M = \frac{1}{2}(V_{c1} - v_{c2}) \quad (4)$$

The partial voltage equilibrium (Vc1; Vc2) across C1 and C2 is obtained by the addition of the subsequent zero fraction by the balance control of the voltage F (s) to the current references shown in Figure 8 and represented in Equation (5).

$$\begin{aligned} i_a^* &= I_a^* + i_0 \\ i_b^* &= I_b^* + i_0 \\ i_c^* &= I_c^* + i_0 \end{aligned} \quad (5)$$

The addition of the zero sequence does not have a direct impact on the formation of large pipelines but also contributes to the timing of changing conditions.

2.3. Selection of Inductor

The value of filter inductor is calculated based on switching frequency, current ripple and required DC output Voltage.

$$L = \frac{\mathrm{Vdc} * \sqrt{3} * \mathrm{M} * \left(1 - \mathrm{M}\frac{\sqrt{3}}{2}\right)}{\mathrm{f_s} * 4 * \Delta i_l} \quad (6)$$

where,

V_{dc} = DC output voltage

M = Modulation index = (V_{ph} peak)/(0.5*V_{dc})

F_s= Switching frequency

$\Delta_{iL,,pp,\ max}$ = Maximum allowable ripple in inductor current.

2.4. Loss Estimation

Loss of power on any semiconductor device includes loss of performance and loss of switching [2]. Loss of IGBT and Diode performance is estimated using the

following formula:

$$P_{con\,IGBT} = \frac{1}{T_{sw}}\int_0^{T_{sw}} P(t)dt = = U_{ce0} \cdot I_{cav} + I^2_{crms} \cdot r_c$$

$$P_{con\,Diode} = \frac{1}{T_{sw}}\int_0^{T_{sw}} P(t)dt = = U_{D0} \cdot I_{Dav} + I^2_{Drms} \cdot r_D \quad (7)$$

where U_{ce0}, r_D, U_{D0},r_c are obtained from output characteristics of device data sheet.

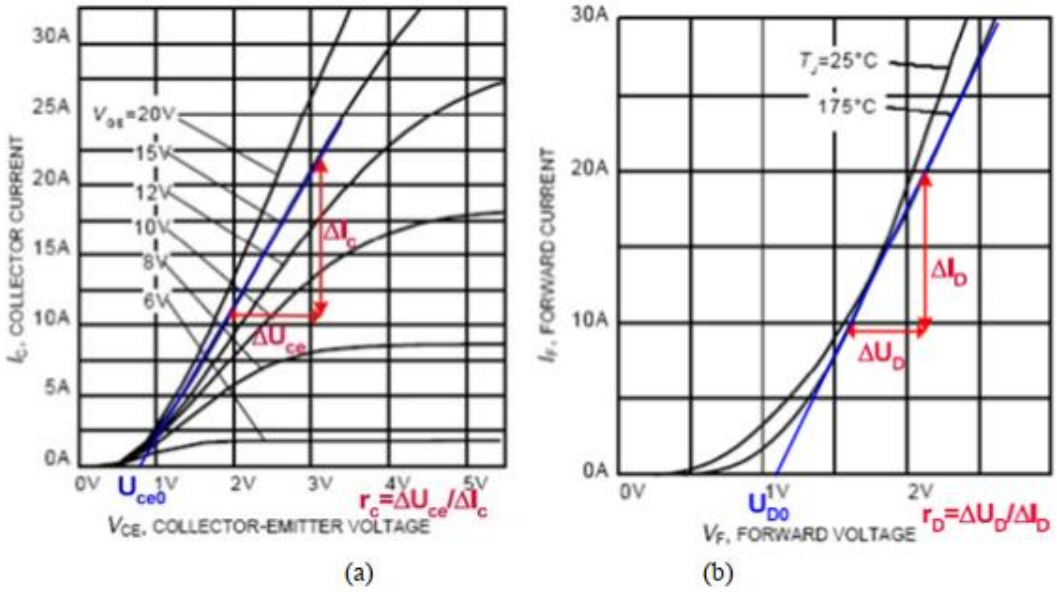

Figure 6: Output characteristics of (a) IGBT (b) Diode

Average and RMS values of currents for Vienna Rectifier topologies are calculated by using formula as presented in Table 4. [6]

Table 4: Average and RMS Current Calculation

$M=\frac{V_{ph\,peak}}{\frac{1}{2}V_{dc}}$		Topology 1		Topology 4	
		Average quantity	RMS quantity	Average quantity	RMS quantity
Active Switch		$I_{Rmax}\left(\frac{1}{\pi}-\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$	$I_{Rmax}\left(\frac{1}{\pi}-\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
Diode	D1, D2	$I_{Rmax}\left(\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{2M}{3\pi}}$	$I_{Rmax}\left(\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{2M}{3\pi}}$
	D3, D4	$I_{Rmax}\left(\frac{1}{\pi}\right)$	$I_{Rmax}\left(\frac{1}{2}\right)$	-	-

Switching loss is calculated by using following formula,

$E_{sw} = E_{on}+E_{off}$ for IGBT and
$E_{sw} = E_{rr}$ for Diode

$$E_{sw} = E_{swref} \cdot \left[\frac{I}{I_{ref}}\right]^{Ki} \left[\frac{V}{V_{ref}}\right]^{Ki} \cdot \left(1 + TC_{sw}\left(T_j - T_{jref}\right)\right) \quad (8)$$

where I_{ref} , V_{CCref}, T_{jref} and E_{swref} are the nominal test conditions.

Ki: Current Dependency Exponent

(IGBT ~ 1; FWD ~ 0.5… 0.6)

Kv: Exponent of power dependency

(IGBT ~ 1.2… 1.4; FWD ~ 0.6)

TC: Temperature coefficient for changing losses

(IGBT ~ 0.003; FWD ~ 0.005… 0.006)

The number of module losses combined with the operation and switching losses are calculated in Topology 1 & 4 with a switching frequency of 15 kHz shown in Figure 7 and Figure 8 severally**.**

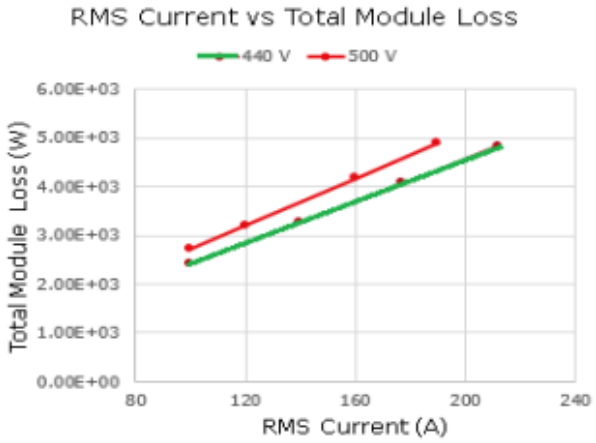

Fig.7. Total module loss of Topology 1

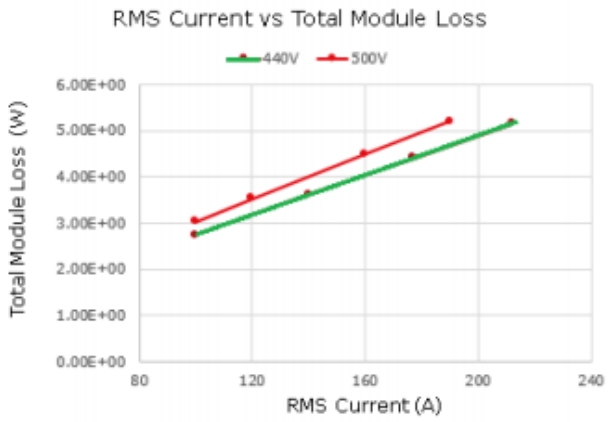

Fig.8. Total module loss of Topology 4

From the above loss estimation, the module losses are less for Topology 1 when compared with Topology 4.

3. Result and Discussion

3-Phase simulation model, 3-Level Vienna rectifier for Topology 1 with required specifications with hysteresis control technique is implemented in MATLAB/SIMULINK is shown in Figure 9.

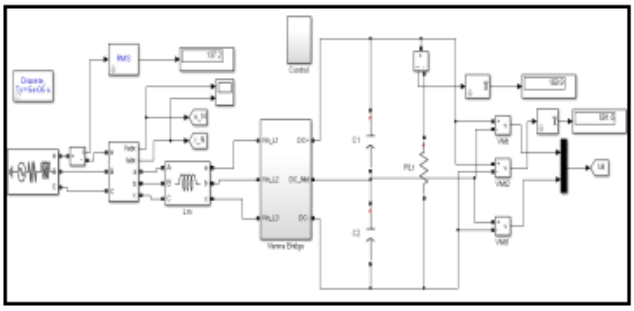

Fig.9. Vienna Rectifier with Hysteresis Control

Input power with current waves, output voltage, and current THD output from 30A to 230A Vienna 440V and 500V converter is shown in Figure 10, Figure 11, and Figure 12 respectively. Figure 10 shows that the input voltage and current are in each phase thus gaining the element of the coupling force and the current input is sinusoidal. Figure 11 shows that a fixed dc voltage of 591 volts is found at the outlet. It is found in Figure 12 that the output current is over 100A where the current THD is less than 5% and satisfies the Power Level Levels thus can be used as an end-to-end converter and high power drives.

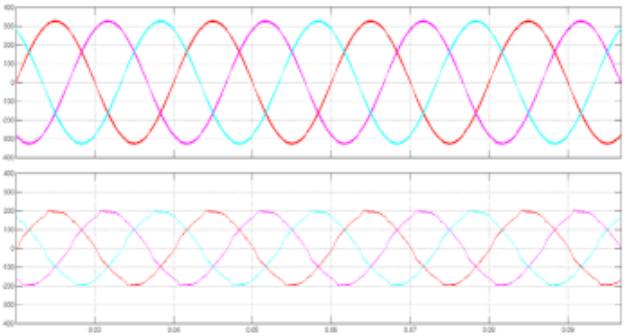

Fig.10. Power input and current waves

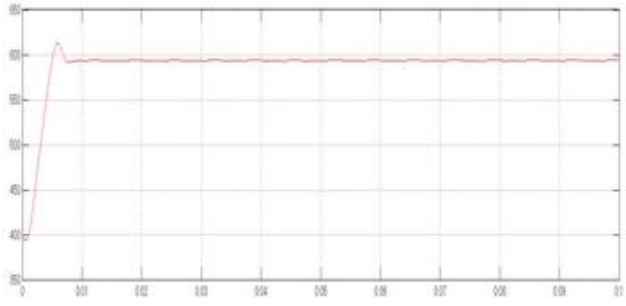

Fig.11. Output Voltage waveforms

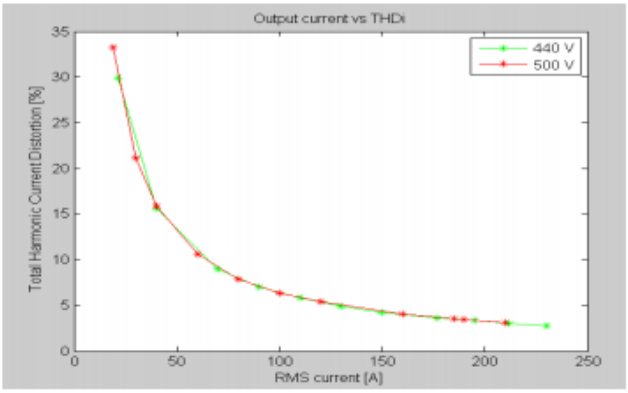

Fig.12. THD variation with Current

4. Conclusion

This paper developed a third phase ac / dc modifier based on three levels of bidirectional-switch Vienna topologies are compared and found that Topology 1 has more advantages like lower module loss, low device ratings, and easy availability of modules. Power circuit design is made for a 90kW drive. The simulation has been implemented using a hysteresis-based control strategy with a closed-loop in Mat lab / SIMULINK for a 90 kW, input supply voltage of 400 V, 50 Hz and the DC link voltage is maintained at 591V(3% boost in line peak voltage). The simulation results show that Vienna Rectifier satisfies all the requirements of the frontend of electric drive thus showing triple-fold performance like harmonic compensation, power factor correction, and rectification and achieves,

• Amplitude load flow

• Integration energy element and

• Source current THD < 5%.

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