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Received: 26.01.2021 Revised: 11.02.2021 Accepted: 24.02.2021

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Research Article

Modelling, Simulation and Analysis of Three Phase/Level Vienna Rectifier as a Front end Converter

P. Sweety Jose[*1], P.Subha Hency Jose[2], K. Bhagya Lakshmi[1]

[1] *Department of EEE, PSG college of Technology, Coimbatore, India.*

[2] *Department of EIE, Karunya University, Coimbatore, India.*

A three-phase front end ac to dc rectifier based on Vienna Rectifier with a three phase/level bidirectional switch topology is presented here. Various topologies of Vienna Rectifier were analyzed and selection of best topology for the front end of Low Harmonic Electric drives is reported. The comparative study has been done among 5 topologies with respect to number of semiconductor devices, semiconductor losses, number of gate drivers etc. Six switch Vienna Rectifier topology 1 is found to be the best solution for harmonic mitigation in the front end of Low harmonic Drives. Power circuit design is made for 90 kW drive and Hysteresis based closed loop control strategy is implemented. The simulation has been implemented in MATLAB/SIMULINK for a 90 kW Vienna Rectifier for input supply voltage of 400 V, 50 Hz and the DC link voltage is maintained at 591V(3% boost in line peak voltage). The simulation result shows that sinusoidal input current, unity power factor is achieved and the current THD is limited to less than 5% as per IEEE 519-2014 standard.

Keywords: Vienna Rectifier, Three level converters, Topologies, Hysteresis control, Power Circuit Design, THD and Power loss.

1. Introduction

Generally, ac-to-dc power converters can be classified into two types as line commutated also called as passive rectifiers and self-commuted rectifiers which are known as active or Pulse Width Modulation (PWM) rectifiers. The passive rectifiers, employs diode or thyristor based switches, which undergoes line commutation or switching at the zero crossing of the ac supply currents whereas Active Rectifiers employs semiconductor technologies, such as Insulated Gate Bipolar Transistor (IGBT), Gate Turn-off Thyristor (GTO), Insulated Gate Commutable Thyristor (IGCT), which are capable of actively controlling the ac supply currents[1].

Correspondence should be addressed to
P. Sweety Jose; psj.eee@psgtech.ac.in

Passive rectifiers are inexpensive, highly reliable, and provides good efficiency but they usually inject significant amount of current harmonics at the supply side and requires additional filtering requirements to attain unity power factor and does not meet power quality standards. On the other hand, Active Rectifiers are more expensive, less reliable and has lower efficiency when compared to passive rectifiers [3]. Nevertheless, the Active Rectifiers are most promising from the power quality point of view, as unity power factor and low current Total Harmonic Distortion (THD) can be achieved. The pursuit for a new rectifier which combines the advantages of both passive and active rectifier has lead this area of research to a new group of rectifiers called Vienna Rectifier.

Vienna rectifier is a non-regenerative three-level boost rectifier with Three-phase/level and found to be the best choice with respect to power losses, size of passive components, efficiency, reliability, high power density,

low voltage stress, unity power factor and less current THD which meets International Electro Technical Commission 61000-3-2/61000-3-4 guidelines [4]. The above-mentioned features make Vienna Rectifier a suitable topology for medium and high power application [2].

Design of a 90 kW, Three-phase/level Vienna rectifier is implemented which characterizes sinusoidal input current, less than 5% current harmonic distortions at the supply side and unity power factor. The various topologies of Vienna rectifier, comparison and selection of best topology and the power circuit design including an optimized design procedure, device selection, control technique, selection of Inductor and loss estimation is presented.

2. Topologies of Vienna Rectifier

The Vienna rectifier is derived from the series connection of uncontrolled diode bridge rectifier and dc-to-dc converter. Figure 1 shows the basic topology of Vienna rectifier. Each phase leg consists of six fast recovery diodes (D1-D6), six line frequency diodes (Da-Df) and six switches (Sa-Sf).

Chen et al [12] suggested a methodology for learning multi-scale features at every pixel location in a soft manner. A contemporary semantic image segmentation model is utilized for combined training of multi-scale input images besides attention model. As well, with extra supervision to output at every scale is crucial for attaining outstanding performance after multi-scale features integration. Three interesting datasets, containing PASCAL-Person-Part, PASCAL VOC 2012 and a subset of MS-COCO 2014 are utilized for demonstrating model efficacy by carrying out extensive experiments.

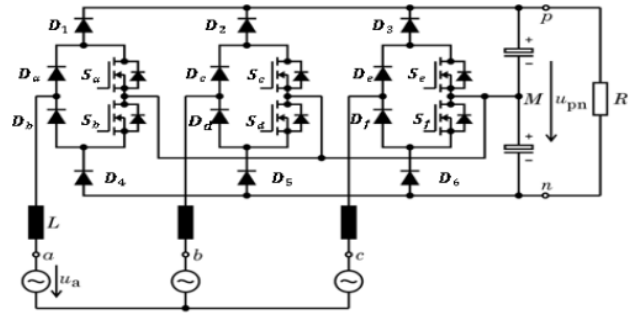

Fig. 1. Topology 1

Alternate phase leg implementations of Vienna Rectifier are shown in Figure 2.

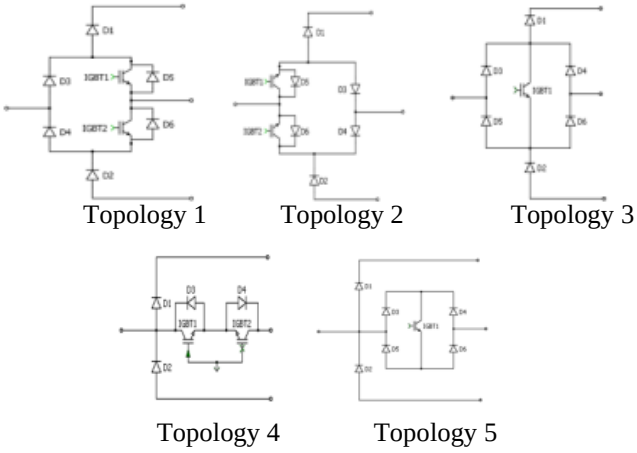

Fig. 2. Various Topologies of Vienna Rectifier

Table 1: Comparison among various Topologies of Vienna Rectifier

S.No	Parameter		Topology 1	Topology 2	Topology 3	Topology 4	Topology 5
1	No of diodes		12	12	18	6	18
2	No of IGBT's (S_a)		6	6	3	6	3
3	Total Device count		18	18	21	12	21
4	Blocking voltage of diodes	recovery	Vdc/2	Vdc/2	Vdc/2	Vdc/2	Vdc/2
		frequency	-	-	Vdc/2	-	Vdc/2
5	Blocking voltage of switches		Vdc/2	Vdc/2	Vdc/2	Vdc/2	Vdc/2
6	No. of Gate drivers / phase leg		2	2	1	1	1
7	Hardware Realization		Moderate	Moderate	Difficult	Less	Difficult
8	No. of stray inductances in commutation loop		4	4	5	4	5
9	Over voltage spikes		Less	Less	more	Less	More
10	+ive /-ive clamping path		Diode *2	Diode + MOSFET	Diode *2	Diode	Diode *2
11	Middle point clamping path		Diode + MOSFET	Diode + MOSFET	Diode*2+MOSFET	MOSFET *2	Diode*2+MOSFET
12	Devices in commutation		Ex.Diode+MOSFET	Ex.Diode+MOSFET	Ex.Diode+MOSFET	Ex.Diode+MOSFET	Ex.Diode+MOSFET

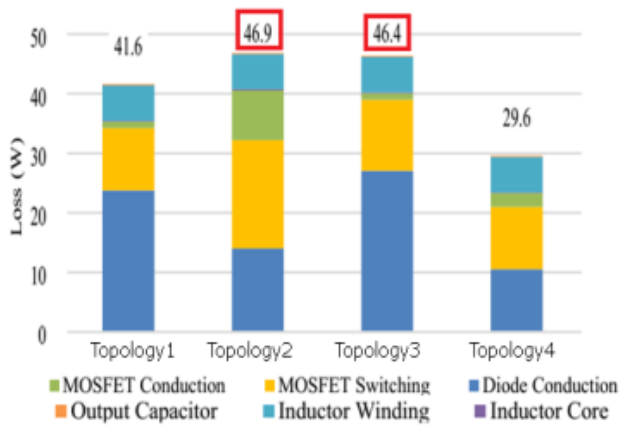

Fig. 3. Loss Comparison

From Figure 3, the losses in topology 2 and 3 is more. Topology 5 is similar to Topology 3 but the two diodes D1 & D2 in each leg are rated for full DC output voltage, where as in topology 3 these are rated for half of the DC output voltage. So, the losses in Topology 5 are normally more than Topology 3. Finally, topologies 2, 3 and 5 are eliminated and the topologies 1& 4 are considered for further analysis [5], [1].

3. Power Circuit Design

The specifications for the design of 3-phase, 3-level rectifier has been shown in Table 2. Assumptions made are the input current to be a pure sinusoid and the rectifier to be operating at UPF with Efficiency of 98 %.

Table 2: Specifications

Quantity	Rating
Output DC power	90 kW
Input 3Ø AC line-line voltage	(380-15% of 380) to (500+10% of 500) V
Frequency of input voltage	50 Hz
Switching Frequency	20 kHz
Output DC voltage	591 V (1.03*Vline peak)

3.1. Design Procedure

The design procedure is described graphically via the flow chart diagram in Figure 4. Initially the converter specifications are defined followed by the selection of the modulation scheme. In order to obtain an optimal design the sweeping program is executed. All the passive devices like input boost inductors, DC bus capacitors are designed (mainly constrained by power quality standard) and their loss estimation for conduction loss and switching loss was done accordingly based on the switching frequency selection. The semiconductor device selection achieving lowest loss will be the optimized design at this switching frequency. By sweeping for different switching frequencies, the relationship between optimized size of passive components and losses can be obtained [4].

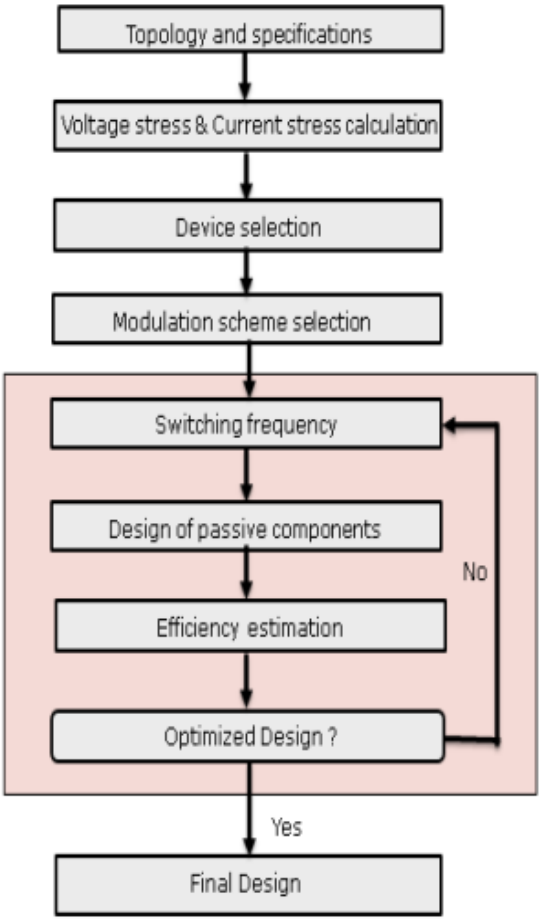

Fig.4. Optimization Procedure

3.2. Device Selection

Voltage stress of the device is calculated by considering maximum value of input supply voltage i.e., 500+10% of 500 therefore, V = 550 V. For both the topologies, voltage stress of IGBT is half of the DC output voltage. Voltage stress of all diodes in topology 1 is half DC output voltage and for topology 4, diodes D1&D2 are rated for full DC voltage and D3 & D4 are rated for half of the DC output voltage [6].

The nominal overload current of 90 kW drive used in industries is 212 A. Current stress of devices is calculated by considering peak value of nominal overload current. The device selection for Topology 1 & 4 is presented in Table 3.

Table 3: Device Selection

Parameter	Topology1		Topology4		
	IGBT	D1 – D4	IGBT	D1 & D2	D3 & D4
Voltage Stress(V)	481	481	481	962	481
Voltage Rating(V)	650	650	650	1200	650
Current Stress (A)	330	330	330	330	330
Current Rating(A)	400	400	400	400	400
Module	F3L400R07ME4_B22		F3L400R12PT4_B26		

3.3. Control Technique

The Hysteresis based control strategy is implemented for the 3-phase, 3-level Rectifier and is shown in Figure 5. The control of the rectifier output and the wave-shaping of input line current is performed by the use of individual hysteresis controllers [7], [8]. The generation of current reference for unity power factor is obtained by multiplying the output of the voltage controller G(s) with sine wave of unit amplitude and in phase with the input voltage as given in the equation (1).

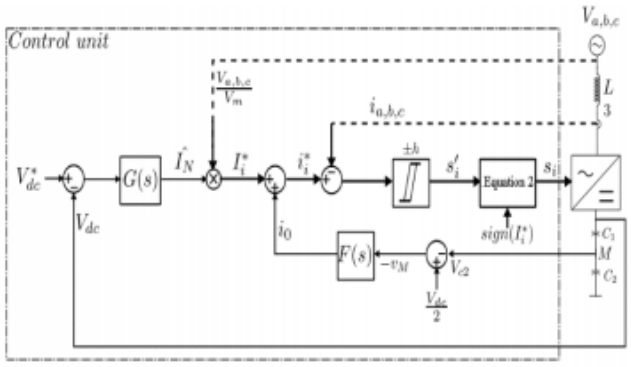

Fig.5. Hysteresis based control strategy

$$I_i^* = I_N \frac{V_{i(i=a,b,c)}}{V_m} \quad (1)$$

For generating the control signals, the dependency of the rectifier input voltage on the sign of the input current is taken into consideration by an inversion as given in equation (2).

$$S_i = \begin{cases} S_i' & if\ i_i^* \geq 0 \\ NOT\ S_i' & if\ i_i^* < 0 \end{cases} \quad (2)$$

The control of mains current is obtained by control of the voltage difference across the inductor (L). The error in the current control is limited to the twice the value of the hysteresis band (2h) and the switching signals for IGBT's are obtained from equation (3).

$$S_i' = \begin{cases} 0 & if\ i_i \geq i_i^* + h \\ 1 & if\ i_i < i_i^* - h \end{cases} \quad (3)$$

In addition to the control of mains current, balancing of the DC bus voltage is also essential across the capacitors C1 and C2. The imbalance in the DC bus voltages is due to the loading of DC bus neutral point M by low frequency AC current and this is characterized by the difference in voltage across the capacitors as given in equation (4).

$$v_M = \frac{1}{2}(V_{c1} - v_{c2}) \quad (4)$$

The balance of partial voltages (Vc1; Vc2) across C1 and C2 is obtained by addition of a zero-sequence component by a voltage balance controller F(s) to the current references as shown in Figure 8 and is represented in Equation (5).

$$\begin{aligned} i_a^* &= I_a^* + i_0 \\ i_b^* &= I_b^* + i_0 \\ i_c^* &= I_c^* + i_0 \end{aligned} \quad (5)$$

The addition of a zero sequence component has no direct effect on the shape of mains current but it has impact on the duration of the switching states.

3.4. Selection of Inductor

The value of filter inductor is calculated based on switching frequency, current ripple and required DC output Voltage.

$$L = \frac{Vdc * \sqrt{3} * M * \left(1 - M\frac{\sqrt{3}}{2}\right)}{f_s * 4 * \Delta i_l}$$

where,

V_{dc} = DC output voltage

M = Modulation index = (Vph peak)/(0.5*Vdc)

F_s= Switching frequency

$\Delta_{iL,,pp,\ max}$ = Maximum allowable ripple in inductor current.

3.5. Loss Estimation

Power loss in any semiconductor device consists of conduction losses and switching losses [2]. The

conduction losses for IGBT and Diode are estimated by using the following formula:

$$P_{con\,IGBT} = \frac{1}{T_{sw}}\int_0^{T_{sw}} P(t)dt = = U_{ce0}\cdot I_{cav} + I^2_{crms}\cdot r_c$$

$$P_{con\,Diode} = \frac{1}{T_{sw}}\int_0^{T_{sw}} P(t)dt = = U_{D0}\cdot I_{Dav} + I^2_{Drms}\cdot r_D$$

where U_{ce0}, r_D, U_{D0}, r_c are obtained from output characteristics of device data sheet.

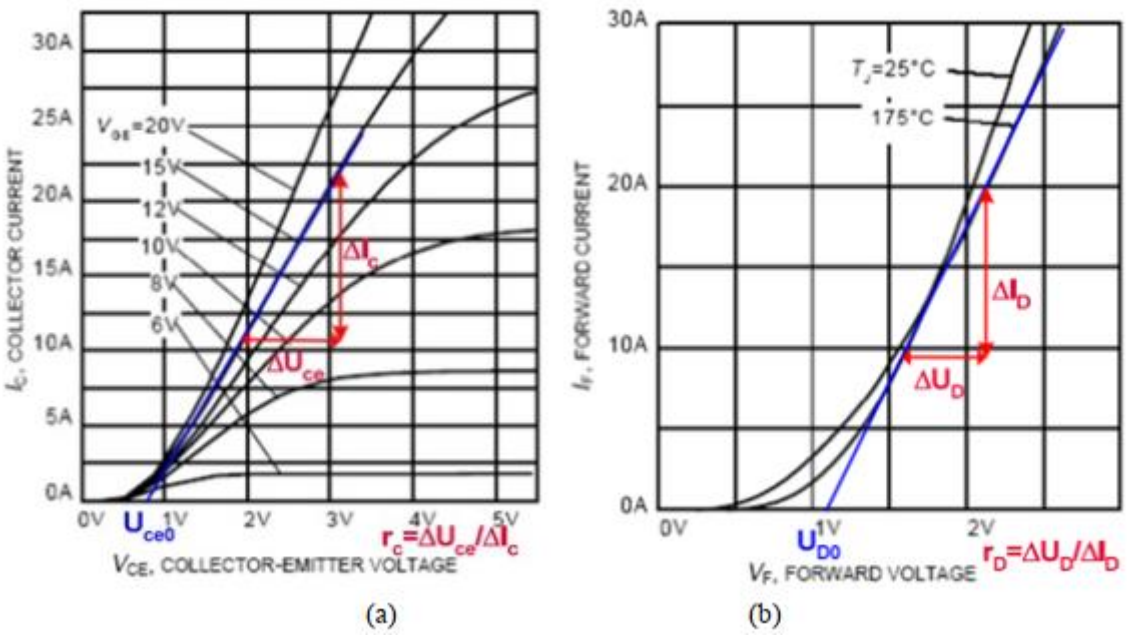

Figure 6: Output characteristics of (a) IGBT (b) Diode

Average and RMS values of currents for Vienna Rectifier topologies are calculated by using formula as presented in Table 4. [6]

Table 4: Average and RMS Current Calculation

$M=\frac{V_{ph\,peak}}{\frac{1}{2}V_{dc}}$		Topology 1		Topology 4	
		Average quantity	RMS quantity	Average quantity	RMS quantity
Active Switch		$I_{Rmax}\left(\frac{1}{\pi}-\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$	$I_{Rmax}\left(\frac{1}{\pi}-\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
Diode	D1, D2	$I_{Rmax}\left(\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{2M}{3\pi}}$	$I_{Rmax}\left(\frac{M}{4}\right)$	$I_{Rmax}\sqrt{\frac{2M}{3\pi}}$
	D3, D4	$I_{Rmax}\left(\frac{1}{\pi}\right)$	$I_{Rmax}\left(\frac{1}{2}\right)$	-	-

Switching loss is calculated by using following formula,

$E_{sw} = E_{on}+E_{off}$ for IGBT and
$E_{sw} = E_{rr}$ for Diode

$$E_{sw} = E_{swref}\cdot\left[\frac{I}{I_{ref}}\right]^{Ki}\left[\frac{V}{V_{ref}}\right]^{Ki}\cdot\left(1+TC_{sw}\left(T_j - T_{jref}\right)\right)$$

where I_{ref} , V_{CCref}, T_{jref} and E_{swref} are the nominal test conditions.

Ki: Exponent of current dependency (IGBT~1; FWD~0.5…0.6)

Kv: Exponent of voltage dependency (IGBT~1.2…1.4; FWD~0.6)

TC_{sw}: Temperature coefficient of switching losses (IGBT~0.003; FWD ~0.005…0.006)

The total module loss including conduction and switching loss is calculated for Topology 1& 4 for the switching frequency of 15 kHz is shown in Figure 7 and Figure 8 respectively.

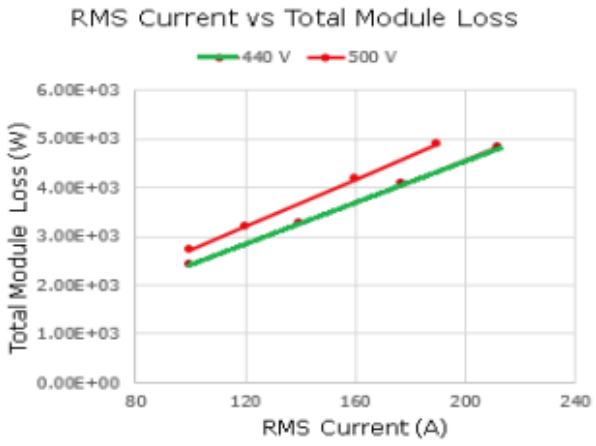

Fig.7. Total module loss of Topology 1

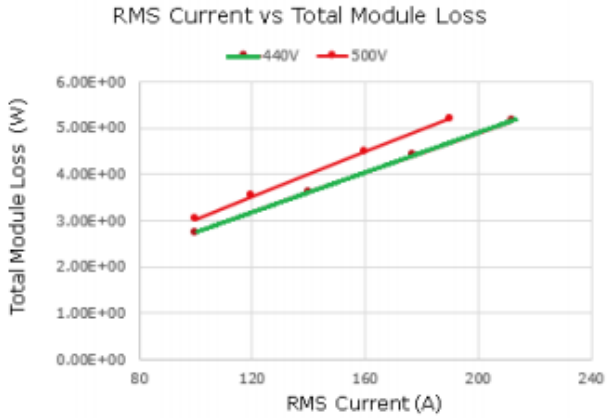

Fig.8. Total module loss of Topology 4

From the above loss estimation, the module losses are less for Topology 1 when compared with Topology 4.

4. Result and Discussion

The simulation model of 3-Phase, 3-Level Vienna rectifier for Topology 1 with required specifications with hysteresis control technique is implemented in MATLAB/SIMULINK is shown in Figure 9.

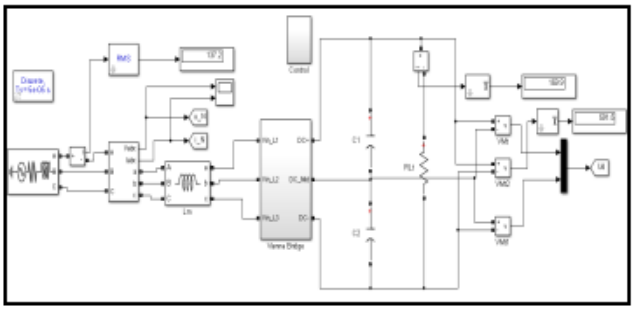

Fig.9. Vienna Rectifier with Hysteresis Control

The input voltage and current waveforms, output voltage and input current THD performance for output currents varying from 30A to 230A of Vienna rectifier for 440V and 500V is shown in Figure 10, Figure 11 and Figure 12 respectively. Figure 10 shows that the input voltage and current are in phase with each other thus achieving unity power factor and input current is sinusoidal. Figure 11 shows that a constant dc voltage of 591 volt is obtained at the output. It is found from Figure 12 that for output currents above 100A the current THD is less than 5% and satisfies Power Quality Standards thus could be used as front-end converter for medium and high power drives.

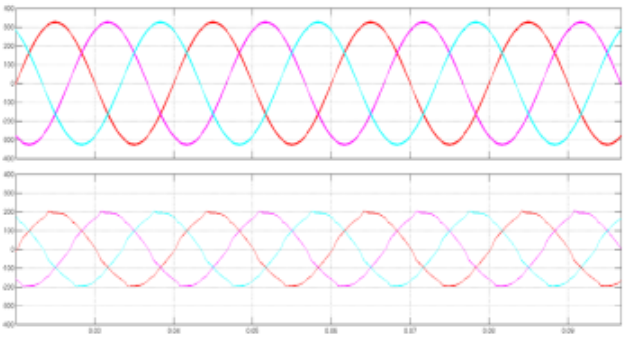

Fig.10. Input Voltage and Current waveforms

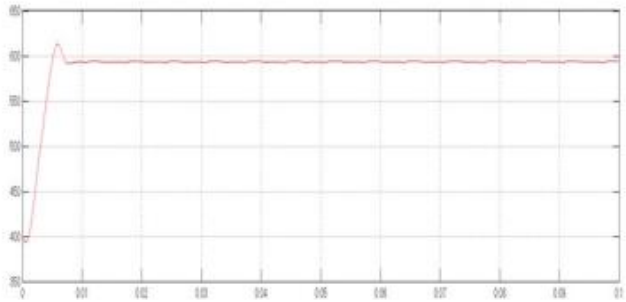

Fig.11. Output Voltage waveforms

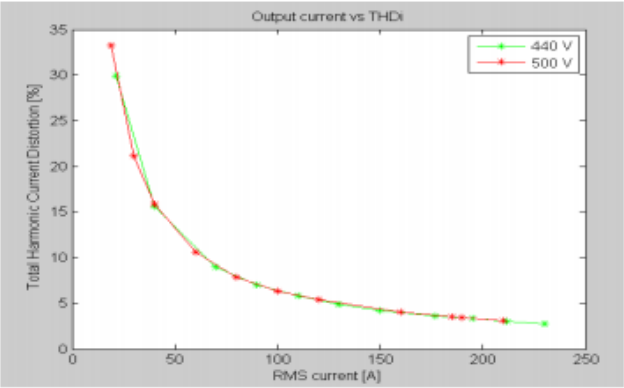

Fig.12. THD variation with Current

5. Conclusion

In this paper optimized front-end three-phase ac/dc rectifier based on the three-level bidirectional-switch Vienna topologies are compared and found that Topology 1 has more advantages like lower module loss, low device ratings and easy availability of modules. Power circuit design is made for 90 kW drive. The simulation has been implemented using Hysteresis based control strategy with closed loop in MATLAB/SIMULINK for a 90 kW, input supply voltage of 400 V, 50 Hz and the DC link voltage is maintained at 591V (3% boost in line peak voltage). The simulation results show that Vienna Rectifier satisfies the all the requirements of front end of electric drive thus showing triple fold performance like harmonic compensation, power factor correction and rectification and achieves,

- Sinusoidal input current
- Unity power factor and
- Source current THD < 5%.

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